FIG. 1

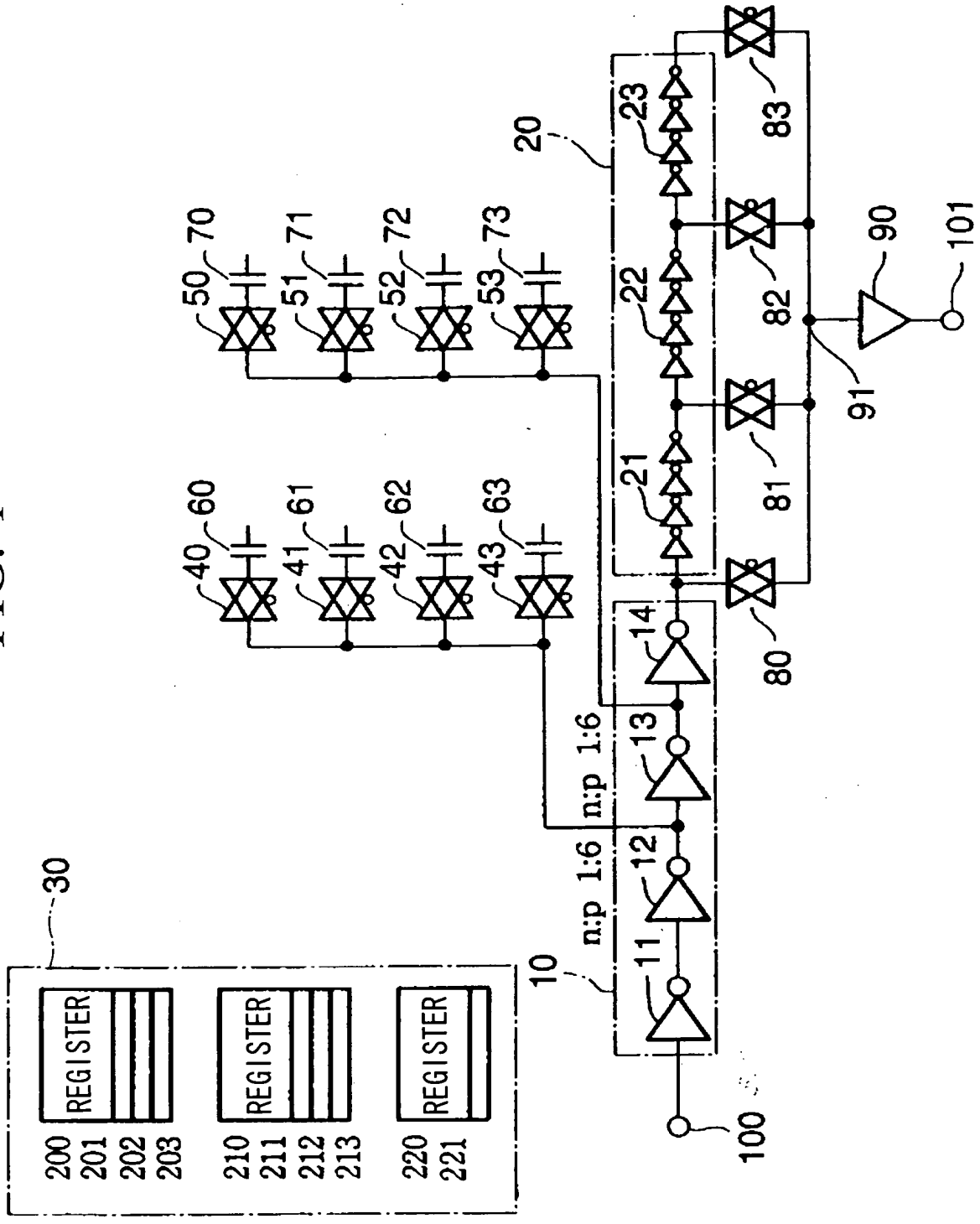

REGISTER
REGISTER
REGISTER
200
201
202
203
210
211
212
213
220
221
30
10
20
n:p 1:6
n:p 1:6
11
12
13
14
21
22
23
40
41
42
43
50
51
52
53
60
61
62
63
70
71
72
73
80
81
82
83
90
91
100
101

FIG. 2

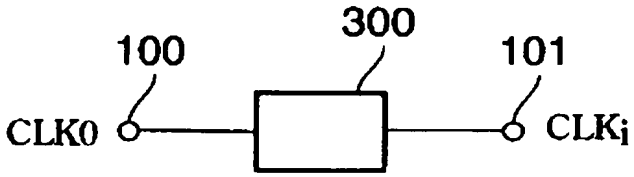


FIG. 4

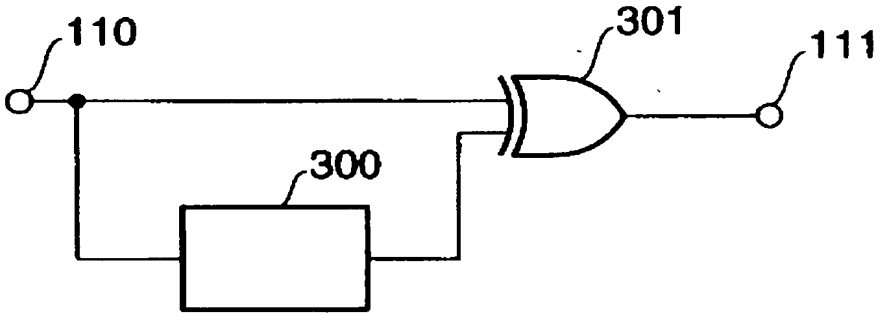
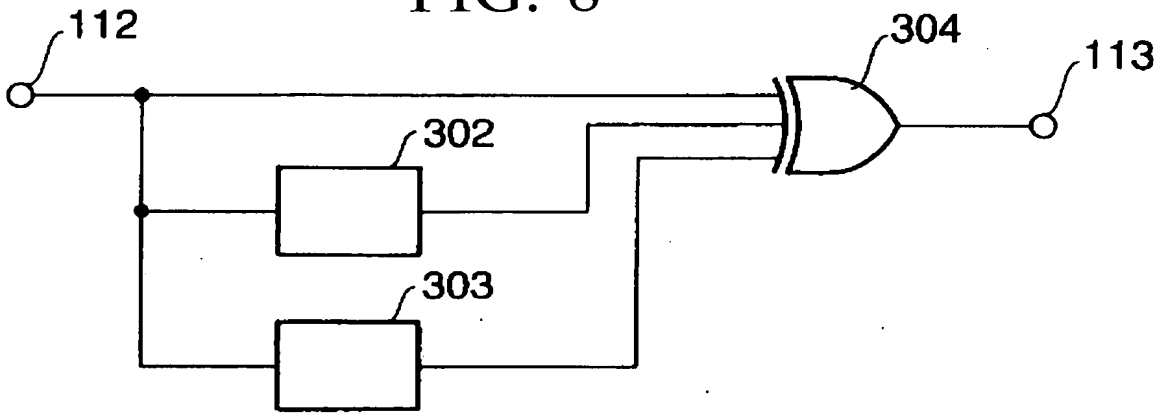


FIG. 8



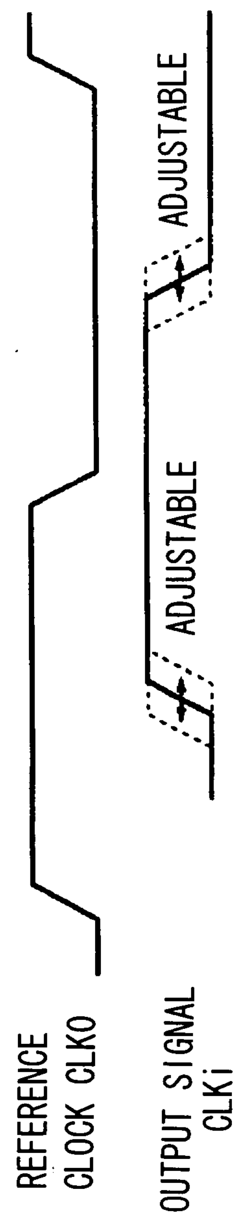


FIG. 3A

FIG. 3B

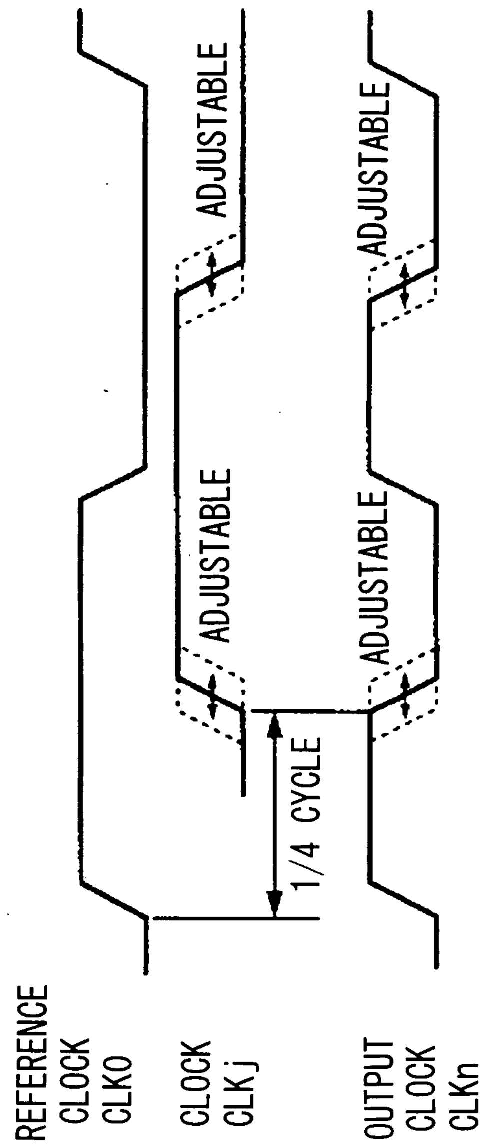


FIG. 5A

FIG. 5B

FIG. 5C

FIG. 6A

FIG. 6B

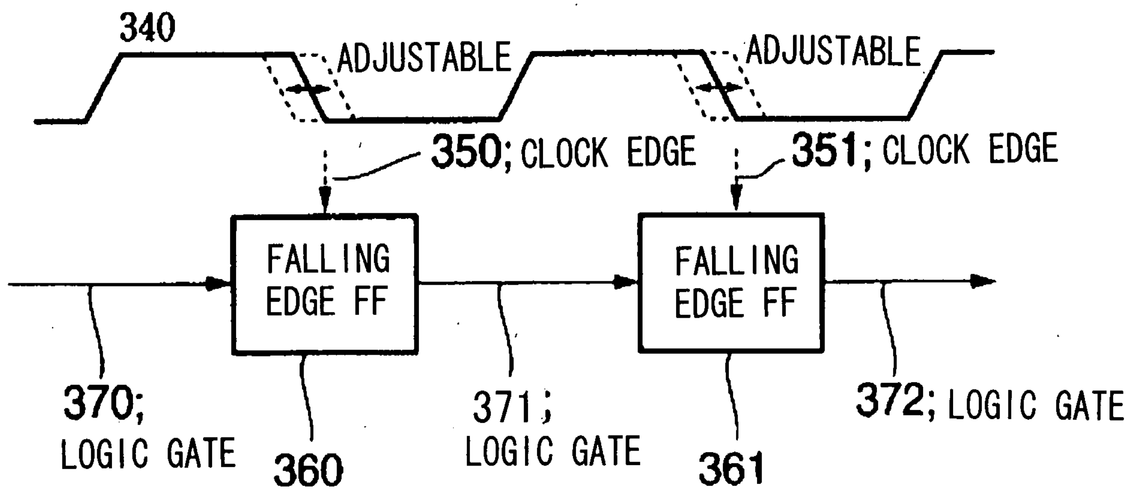
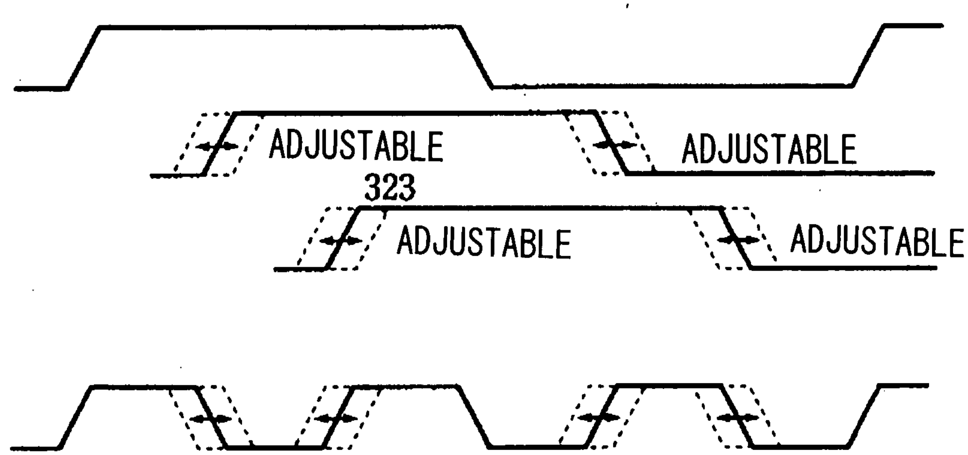


FIG. 9A REFERENCE CLOCK CLK0

FIG. 9B CLOCK CLKx

FIG. 9C CLOCK CLKy

FIG. 9D CLOCK CLKz



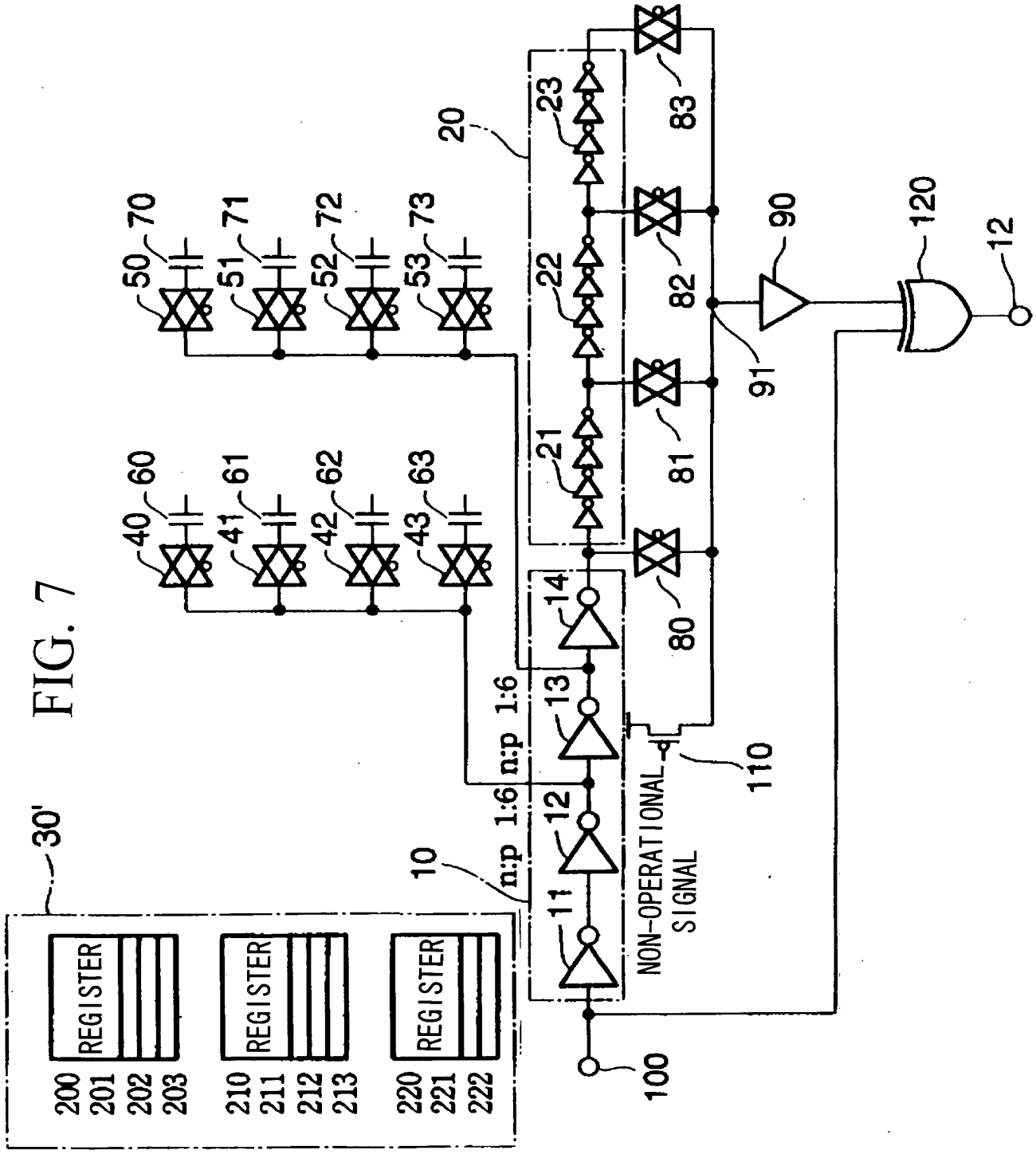

30'
10
REGISTER
REGISTER
REGISTER
200
201
202
203
210
211
212
213
220
221
222
n:p 1:6
n:p 1:6
11
12
13
14
20
21
22
23
40
41
42
43
50
51
52
53
60
61
62
63
70
71
72
73
80
81
82
83
90
91
100
110
120
12
NON-OPERATIONAL
SIGNAL

FIG. 7

FIG. 10

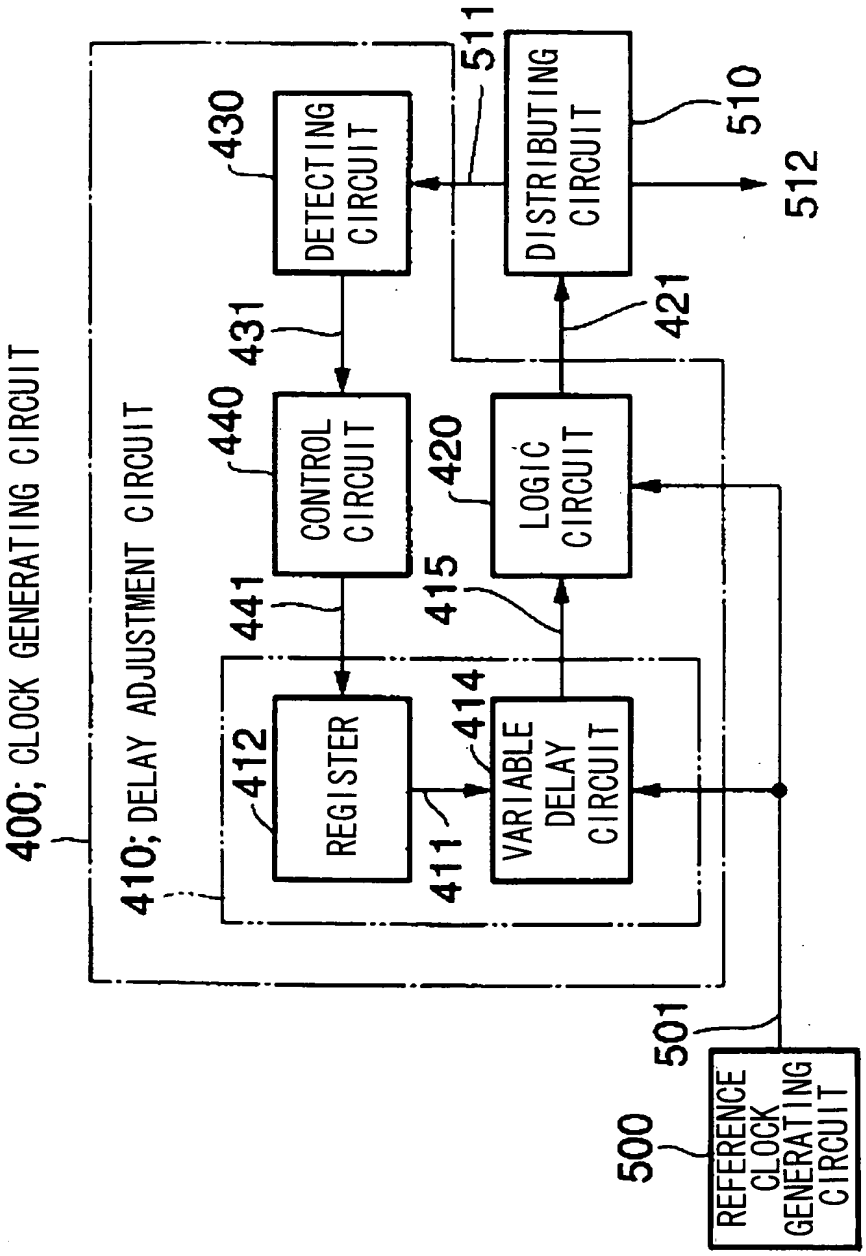

400; CLOCK GENERATING CIRCUIT
410; DELAY ADJUSTMENT CIRCUIT
REGISTER
412
VARIABLE DELAY CIRCUIT
414
411
441
CONTROL CIRCUIT
440
431
DETECTING CIRCUIT
430
415
LOGIC CIRCUIT
420
421
DISTRIBUTING CIRCUIT
511
510
512
501
500
REFERENCE CLOCK GENERATING CIRCUIT

FIG. 11

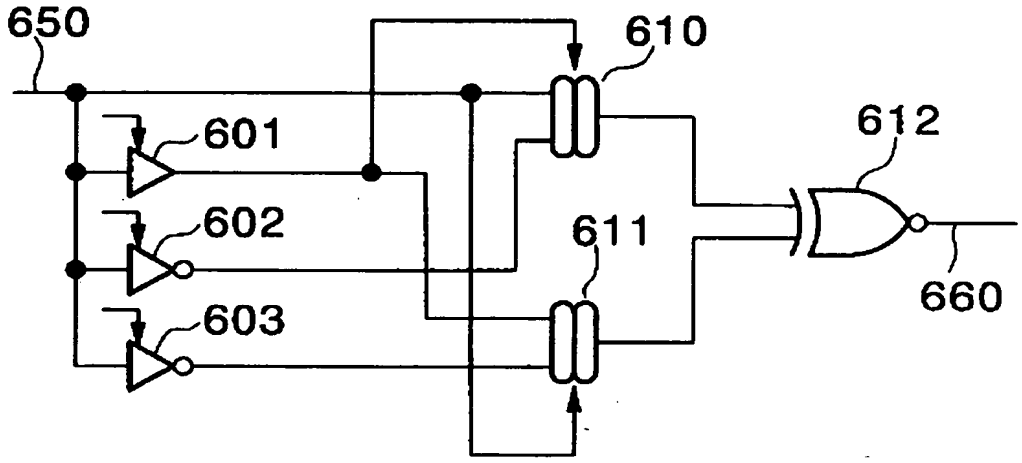

650
610
601
612
602
611
603
660

FIG. 13

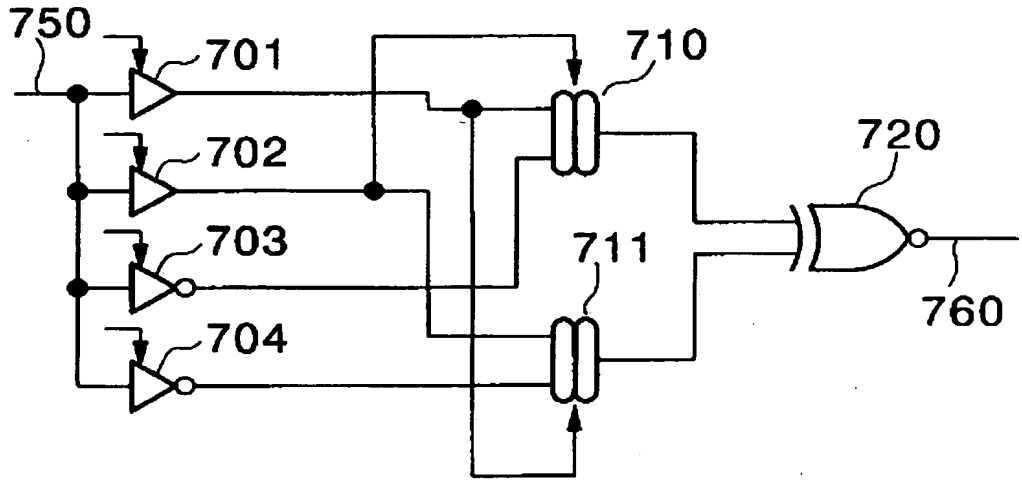

750
701
710
702
720
703
711
704
760

FIG. 12A INPUT SIGNAL 650

FIG. 12B OUTPUT SIGNAL OF 601

FIG. 12C 2/4 CYCLE DELAYED SIGNAL OF 650

FIG. 12D OUTPUT SIGNAL OF 602 3/4 CYCLE DELAYED

FIG. 12E SIGNAL OF INPUT SIGNAL 650

FIG. 12F OUTPUT SIGNAL OF 603

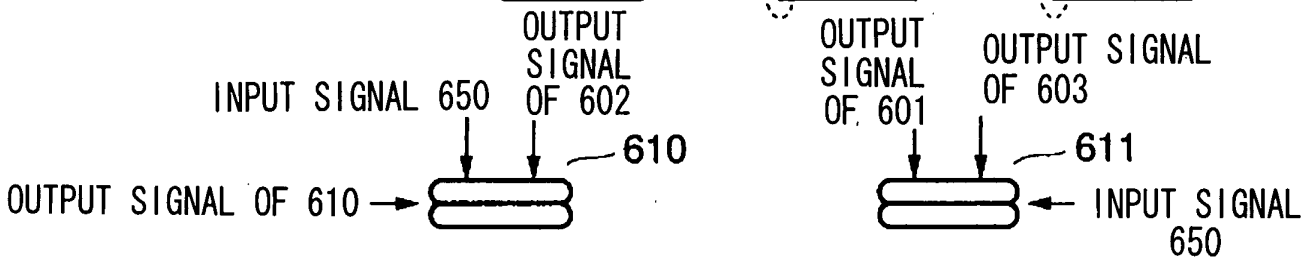


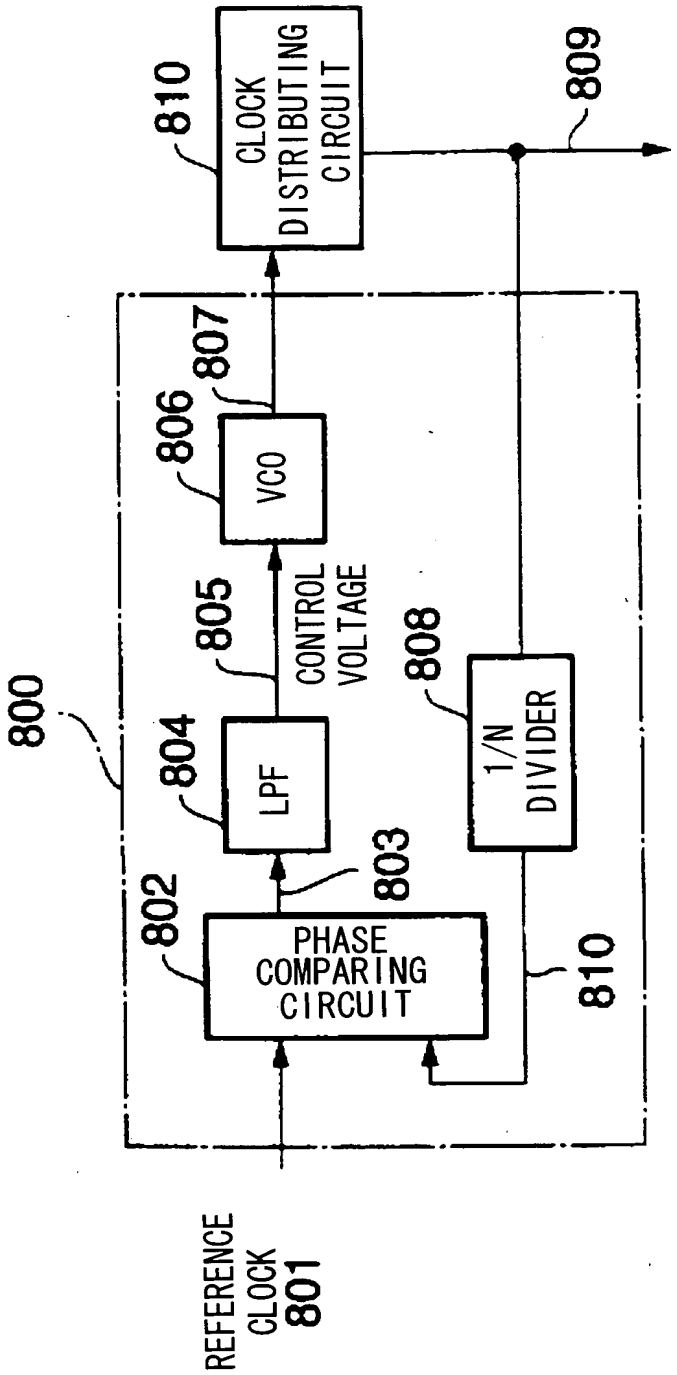
FIG. 12G OUTPUT SIGNAL OF 601

FIG. 12H OUTPUT SIGNAL OF 611

FIG. 12I OUTPUT SIGNAL 660

Title: DELAY ADJUSTMENT CIRCUIT AND A CLOCK GENERATING CIRCUIT USING THE SAME
Inventor(s): Atsushi YOSHIKAWA, et al
Atty. Docket No. 088941/0184
Sheet 8 of 9

FIG. 14


800
CLOCK DISTRIBUTING CIRCUIT
810
809
VCO
806
807
LPF
804
805
CONTROL VOLTAGE
1/N DIVIDER
808
PHASE COMPARING CIRCUIT
802
803
810
REFERENCE CLOCK
801